Amendments to the Claims:

Please amend claims 1, 2, 5, 6, 8, 10, 13-16, and 18-20 as follows:

1. (currently amended) A method for controlling a plurality of data channels connected via a common data bus to a bus controller, the method comprising:

transmitting a message including a command from the bus controller to the plurality of data channels, wherein the message comprises a plurality of bits having a value defined by a transition between first and second states, wherein the message is issued in a serial manner; and

performing a function defined by the command at each of the plurality of the data channels, wherein the data channels are connected to the common data bus in parallel to perform predefined functions as parallel processes to thereby support high speed communication over said common data bus, wherein performing the function comprises commencing performance of the function at each data channel at the same predetermined time using ~~relative to~~ a predetermined transition in the message as a trigger, such that the plurality of data channels can perform the function simultaneously in a time-deterministic manner.

2. (currently amended) A method according to Claim 1 wherein transmitting the message comprises transmitting the message either asynchronously or at a predetermined bit rate independent of an accompanying synchronous clock signals.

3. (original) A method according to Claim 1 wherein commencing performance of the function comprises commencing performance of the function at each data channel coincident with a predetermined transition defined in the message.

4. (currently amended) A method according to Claim 1 wherein transmitting the message comprises transmitting a message including a command from the bus controller to the plurality of data channels, wherein the message comprises a plurality of bits ~~having a value defined by a transition between first and second states~~, wherein the message comprises a sync portion, a message body and a parity bit, and wherein commencing performance of the function comprises commencing performance of the function at each data channel coincident with the transition that defines the value of the parity bit.

5. (currently amended) A method according to Claim 1 wherein transmitting the message comprises transmitting a message comprising a start bit, a command field, an address field ~~filed~~ having an ~~address~~ unused last bit set to 0, and a stop bit set to 1, and wherein commencing performance of the function comprises commencing performance of the function at each data channel coincident with the transition from the address bit to the stop bit.

6. (currently amended) A system for controlling a plurality of data channels connected via a common data bus to a bus controller, the system comprising:

a plurality of network device interfaces adapted to interconnect respective data channels with the bus controller via a common digital bus, wherein the data channels are connected to the common data bus in parallel to perform predefined functions as parallel processes to thereby support high speed communication over said common data bus, wherein each network device comprises:

a receiver for receiving a message from the bus controller via the common digital bus, wherein the message is comprised of a plurality of bits having a value defined by a transition between first and second states and is issued in a serial manner; and

a device interface for providing commands to the associated data channel in response to a message received by said receiver and for receiving data from the associated data channel,

wherein when said device interface of each network device interface receives a selected command from the bus controller, each device interface provides the command to the associated data channel at the same predetermined time using ~~relative to~~ a predetermined transition in the message as a trigger, such that the plurality of data channels can perform the function simultaneously in a time-deterministic manner.

7. (original) A system according to Claim 6 wherein each network device interface further comprises a transmitter for transmitting messages including the data received by said network device interface from a data channel to the bus controller via the common digital bus.

8. (currently amended) A system according to Claim 6 wherein said receiver of each network device interface is capable of receiving the message either asynchronously or at a bit

rate from a predetermined set of bit rates independent of any accompanying synchronous clock signals.

9. (original) A system according to Claim 8 wherein said transmitter of each network device interface transmits messages at the same bit rate that said receiver received the message.

10. (currently amended) A system according to Claim 6 wherein said receiver ~~device interface~~ of each network device interface provides the commands to the associated data channel coincident with a predetermined transition in the message.

11. (original) A system according to Claim 6 wherein said receiver of each network device interface receives messages having a plurality of bits ~~having a value defined by a transition between first and second states~~, wherein the messages comprises a sync portion, a message body and a parity bit, and wherein said device interface of each network device interface provides the commands to the associated data channel coincident with the transition that defines the value of the parity bit of the message.

12. (previously presented) A system according to Claim 6 wherein said receiver of each network device interface receives messages comprised of a start bit, a command field, an address field having an address bit set to 0, and a stop bit set 1, and wherein said device interface of each network device interface provides the commands to the associated data channel coincident with the transition from the address bit to the stop bit.

13. (currently amended) A method for controlling a plurality of data channels connected via a common data bus to a bus controller, the method comprising:

transmitting a message including a command from the bus controller to the plurality of data channels, wherein the message comprises a plurality of bits having a value defined by a transition between first and second states, wherein the message is issued in a serial manner, and wherein the data channels are connected to the common data bus in parallel to perform predefined functions as parallel processes to thereby support high speed communication over said common data bus;

transmitting a synchronous clock signal comprised of a plurality of clock pulses from the bus controller to the plurality of data channels simultaneous with the message; and

performing a function defined by the command at each of the plurality of data channels, wherein performing the function comprises commencing performance of the function at each data channel at the same predetermined time as defined by a respective clock pulse which, in turn, is defined based upon a predetermined relationship to a respective bit of the message, where the respective bit is used as a trigger such that the plurality of data channels can perform the function simultaneously in a time-deterministic manner.

14. (currently amended) A method according to Claim 13 wherein commencing performance of the function comprises commencing performance of the function at each data channel in synchronization with an edge of a first clock pulse following the respective bit of the message.

15. (currently amended) A method according to Claim 13 wherein transmitting the message comprises transmitting a message comprising a plurality of bits having a value defined by a transition between a first state and a second state, wherein the bits of the message define a sync portion, a message body and a parity bit, and wherein commencing performance of the function comprises commencing performance of the function at each data channel at the same predetermined time as defined by a respective edge of a clock pulse which is, in turn, defined based upon a predetermined relationship to the transition that defines the value of the parity bit of the message.

16. (currently amended) A system for controlling a plurality of data channels connected via a common data bus to a bus controller, the system comprising:

a plurality of network device interfaces adapted to interconnect respective data channels with a bus controller via a common digital bus, wherein the data channels are connected to the common data bus in parallel to perform predefined functions as parallel processes to thereby support high speed communication over said common data bus, each network device interface comprising:

a receiver for receiving a message and a synchronous clock signal from the bus controller via the common digital bus, wherein the message is comprised of a plurality of bits having a value defined by a transition between first and second states and is issued in a serial manner, and wherein the synchronous clock signal is comprised of a plurality of clock pulses; and

a device interface for providing commands to the associated data channel in response to a message received by said receiver and for receiving data from the associated data channel,

wherein when said device interface of each network device interface receives a selected command from the bus controller, each device interface provides the command to the associated data channel at the same predetermined time as defined by a respective clock pulse which is defined using ~~based upon~~ a predetermined relationship to a respective bit of the message as a trigger, thereby enabling the data channels associated with the plurality of interfaces to function synchronously.

17. (original) A system according to Claim 16 wherein each network device interface further comprises a transmitter for transmitting messages including the data received by said network device interface from an associated data channel to the bus controller via the common digital bus.

18. (currently amended) A system according to Claim 17 wherein said transmitter of each network device interface transmits messages in either asynchronously on in synchronization with the synchronous clock signal.

19. (currently amended) A system according to Claim 16 wherein said device interface of each network device interface provides the commands to the associated data channel in synchronization with an edge of the first clock pulse following the respective bit of the message.

20. (currently amended) A system according to Claim 16 wherein said receiver receives a message comprising a plurality of bits having a value defined by a transition between a first state and a second state, wherein the bits of the message define a sync portion, a message body

and a parity bit, and wherein said device interface of each network device interface provides the commands to the associated data channel at the same predetermined time as defined by a respective edge of a clock pulse which is, in turn, defined based upon a predetermined relationship to the transition that defines the value of the parity bit of the message.

21. (original) A system according to Claim 16 wherein said receiver receives a message comprising a plurality of bits which are Universal Asynchronous Receiver Transmitter non-return-to-zero encodes, wherein said device interface of each network device interface provides the commands to the associated data channel at the same predetermined time as defined by a respective clock pulse which is defined based upon a predetermined relationship to the transition between the address and stop bits of the message.